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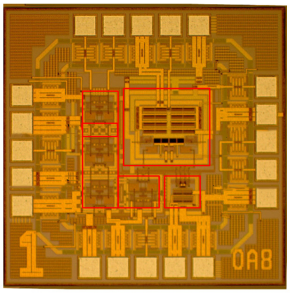
A high-performance CMOS FDMA for pulsed TOF imaging LADAR system



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Abstract: This paper presents a high bandwidth and low noise fully differential main amplifier (FDMA) for pulsed time-of-flight (TOF) imaging laser detection and ranging application (LADAR), which serves to amplify the small pulse echo signal. The cascaded architecture and active inductor technology are used to enlarge the bandwidth of the circuit and reduce the chip area. The cascaded gain stages, which adopted DC offset isolation circuit, are more robust to the alteration of process. A large bandwidth amplifier (LBA) and an output buffer (OB) structure have been designed to enhance the drive capabilities. Besides, in order to adapt the demand of the LADAR system, the amplifier receiver's bandwidth has been limited by using an inter-stage bandpass filter. Implemented in CSMC CMOS technology, the FDMA chip realizes the -3 dB bandwidth of 730.6 MHz, and an open loop gain of 23.5 dB with the bandpass filter worked. The input-referred noise voltage is 2.7 nV/sqrt(Hz), which effectively reduces the system noise. This chip that occupies 0.25 mm×0.25 mm in area consumes a power dissipation of 102.3 mW from the 3.3 V power supply. As a part of the integrated chip of the laser radar system, it can better meet the requirements of system.

Keywords: laser detection and ranging (LADAR) receiver; fully differential main amplifier; cascaded gain stage; active inductor

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应用于脉冲 TOF 成像 LADAR 系统的高性能 CMOS 全差分放大器设计

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摘要：本文设计了一种应用于脉冲飞行时间(TOF)成像激光雷达探测系统的高带宽、低噪声全差分放大器(FDMA)。该芯片采用多级级联结构和有源电感技术，增大电路带宽和减少芯片面积，并且通过使用失调隔离技术，增强了各增益级对工艺偏差的鲁棒性。在输出级电路中，为使全差分放大器具有更强的驱动能力，采用了宽带放大器和输出缓冲器

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级联结构做为输出。同时，为了满足激光雷达系统的实际需求，采用复用失调隔离电路的方式，实现了级间带通滤波来限制放大器的适用带宽。采用 CMSC 的 CMOS 工艺进行了 FDMA 流片。测试结果表明，该芯片具有 730.6 MHz 的-3 dB 带宽，在使用带通滤波器优化后的开环增益为 23.5 dB，等效输入噪声密度为 2.7 nV/sqrt(Hz)，有效地降低了系统噪声。芯片采用 3.3 V 电源供电，功耗为 102.3 mW，整体面积为 0.25 mm×0.25 mm。作为激光雷达全系统集成芯片中的一部分，较好地满足系统指标要求。

关键词：激光雷达接收器；全差分放大器；级联式增益级；有源电感

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1 Introduction

As an optical remote sensing technology, the laser detection and ranging (LADAR) system has been used in many fields[1-3], including the auxiliary driving, intelligent robot for target identification, and the 3D imaging. The pulsed time-of-flight (TOF) LADAR system that measures the distances to targets by emitting and detecting laser echoes accurately has the unique advantage of long detection range compared to other measurement methods such as the continuous-wave optical phase method[4-5].

A block diagram of a typical TOF LADAR system is shown in Fig. 1. As shown in the figure, the LADAR system is composed of a pulsed laser transmitter, an amplifier receiver, a time-to-digital converter (TDC), an analog-digital converter (ADC), and a micro-processor. The pulsed laser transmitter generates a start signal and simultaneously emits an optical pulse signal. After focused by some optical components, the laser pulse signal launches towards the target, and an echo signal will be produced and reflected back when the optical pulse encounters the target. The amplifier receiver, on which this paper focuses, amplify the reflection signal from the target by receiver's optical component to the analog-digital converter, and generates the arrival timing signal (stop) of the echo signal to the time-to-digital converter[6]. In the signal processor, according to the flight time, the distance between the target and the receiver can be calculated through the LADAR formulas by using the micro-processor.

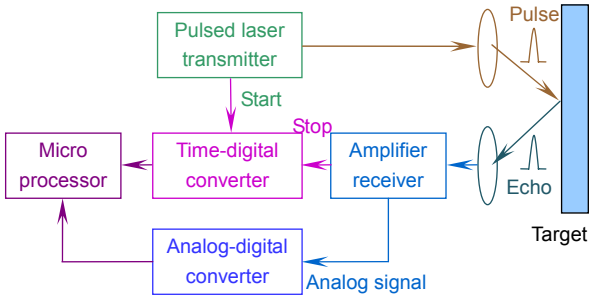

Fig. 1 Block diagram of a typical TOF LADAR

The amplifier receiver which mainly includes a photoelectric detector and analog front-end circuits converts the optical pulse echo signal into an electrical pulse. The photoelectric detector usually employs an avalanche photodiode (APD) because of the high sensitivity. The analog front-end circuits, which mainly consist a trans-impedance amplifier (TIA) and a main amplifier, are used to convert a current signal to a voltage signal for the analog-digital converter and time-to-digital converter to discriminate. However, only by using TIA it cannot satisfy the demand for the remote detection applications. Since the transmit power of the pulse laser are limited, in active imaging system, the performance of the main amplifier becomes a critical issue. Therefore, a high-performance main amplifier is a key component to the LADAR system.

In this paper, a fully differential main amplifier chip has been implemented in a CSMC CMOS process. The proposed amplifier applied active inductor, which is used to reduce the chip area and enlarge the bandwidth of the circuit. In order to apply for LADAR system, this work achieves an inter-stage bandpass filter by reusing the DC offset isolation circuit. Section 2 describes the LADAR system and proposed amplifier receiver. Section 3 introduces the details of fully differential main amplifier. The measurement results of the chip are shown in Section 4, and Section 5 summarizes the design.

2 Proposed amplifier receiver

The amplifier receiver is mainly to amplify the moment of the weak optical echo signal which is come from the target. The input current signal of the photoelectric detector produced can be acquired by the well-known radar principle and responsibility of APD.

$$i_{\rm opt}(R)=R_{\rm APD}\frac{P_{\rm T}\tau_{\rm T}\rho A_{\rm R}}{\pi R_{\rm S}^2}\quad , \tag{1}$$

where $R_{\rm APD}$ is the responsibility of APD, $P_{\rm T}$ is the peak power of the laser transmitted pulse, $\tau_{\rm T}$ is the transmission of the optical system, ρ means the reflection coefficient of the target, $A_{\rm R}$ is the active area of the receiver lens. Last, and $R_{\rm S}$ is the distance between the target and receiver.

Usually, an avalanche PD (APD) is used as the photodetector because of the high responsivity. The gain of a Si

APD can be 50 A/W, but the InGaAs APD has the typical gain of only 10 A/W. Therefore, the minimum detectable echo signal for the receiver will be only few tens of nW by using InGaAs APD.

The signal-to-noise ratio (SNR) can be calculated by the radar formula[7]. In order to suitable the practical applications, the requirement of the SNR is over 5 in the general hundreds of meter detection LADAR system. Further, the SNR over 10 would be advantageous for mm-level accuracy.

Figure 2 shows the block diagram of the proposed amplifier receiver. In Fig. 2, the proposed amplifier receiver consists of two parts: trans impedance amplifier (TIA) and main amplifier. The TIA is an analog circuit that converts the input current pulse signal from the APD into voltage. And the main amplifier's task is to further amplify the small voltage signal to an appropriate level so that the voltage can be process by the followed circuit such as the TDC and ADC. However, only by using TIA it cannot satisfy the demand of the voltage for the remote detection system. Therefore, the performance of the main amplifier influences the optical pulse receiver largely.

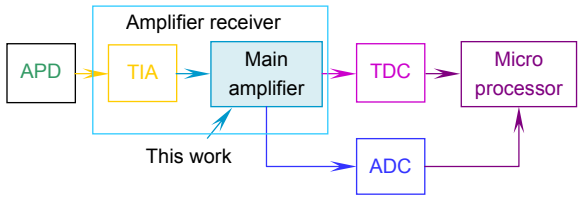

Fig. 2 Block diagram of the proposed amplifier receiver

The main amplifier circuit should have enough wide bandwidth to keep the pulse waveform linearly magnified. However, excessive bandwidth would lead to additional noise entering the receiver, due to the signal-to-noise ratio (SNR) of the receiver deteriorated. The bandwidth (BW) as a critical limit can be approximately expressed as follows[8]:

$$BW \geq \frac{0.35}{t_r} \text{ or } \frac{0.44}{t_r} \quad , \tag{2}$$

where t_r is the rise edge of the time signal. For general applications, the pulsed laser with a peak power of 20 W ~75 W and a width of 3 ns~20 ns is needed[9]. This means that a narrower pulsed echo requires about 100 MHz ~200 MHz BW of the whole receiver channel. In the design, BW of the fully differential main amplifier (FDMA) is demanded over the 500 MHz. At the same time, in order to meet the LADAR system application, this work designs an inter-stage bandpass filter by reusing the DC offset isolation circuit to limit system noise.

3 Circuit description

The structure of the fully differential main amplifier (FDMA) is presented in Fig. 3. In the diagram, the circuit includes four identical gain stages to provide enough voltage gain, a large bandwidth amplifier (LBA) and an output buffer (OB) stage to enhance the deriver ability, and the bandpass filter to limit noise. In order to keep the walk error of the LADAR system small, the bandwidth of amplifier stages must be sufficiently wide frequency range. The stages need to operate linearly and resume rapidly enough after the signal inputting. This circuit is achieved by using several amplifiers chain with a high slew rate and a large bandwidth. However, excessive bandwidth would cause additional noise entering the receiver, which degrades the receiver's signal-to-noise ratio (SNR). Therefore, the bandwidth of the whole amplifier chains should be confined. Meanwhile, the inter-stage bandpass filter which reuses the DC offset isolation circuit to limit system noise and mitigates the problem that the coupled capacitances occupy a large area in CMOS process and lead to attenuate the signal should be carefully designed. In addition, the cascaded gain stage (CGS) that realized by four identical gain stages would deteriorate the amplifiers bandwidth. Therefore, this work adopts the active inductor technology instead of traditional spiral inductor architecture to extend bandwidth. By using the method, the bandwidth of single stage is extend up to 70% without deteriorating the frequency response[10].

In conventional integrated amplifier systems, the cascaded gain stage (CGS) is widely used to achieve optimum results for both high gain and wide bandwidth. Assuming that the circuit consists of n identical gain stages with one pole frequency response, for the multilevel cascaded gain stages, the total bandwidth can be calculated as following (3):

$$BW_{\text{tol}} = BW_{\text{s}} \times (2^{\frac{1}{n}} - 1)^{\frac{1}{2}} \quad , \tag{3}$$

where BW_{s} is the bandwidth of each gain stage, and BW_{tol} is the whole bandwidth of CGS. Therefore, the gain bandwidth product of each gain stage given by (4):

$$GBW_{\text{s}} = \frac{BW_{\text{tol}}}{(2^{\frac{1}{n}} - 1)^{\frac{1}{2}}} \times A_{\text{tol}}^{\frac{1}{n}} \quad , \tag{4}$$

where A_{tol} is the total gain of CGS, and GBW_{s} is the gain bandwidth product of each gain stage.

According to above formulas, there are shown that the increasing number of the gain stages can directly achieve

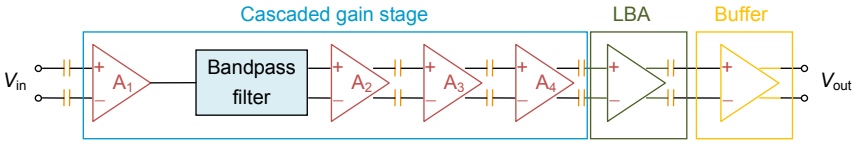

Fig. 3 The architecture of fully differential main amplifier

higher gain. Consequently, the simplest way to enlarge the cascaded gain bandwidth product is to make the number of stages as larger as possible. However, this approach will not only result in a significant increase in the power consumption and area, but also make a rapid accumulation of noise from the gain stage, which has a significant impact on the amplifier circuit stability. In the practical design, the maximum number of stages is usually limited to below five[11].

In the designed pulsed TOF imaging LADAR system, the proposed FDMA needs to meet the requirements as following: $G_{\rm tol}=20\log(A_{\rm tol})\geq 20$ dB , $BW_{\rm tol}\geq 600$ MHz . For n=4, it can be calculated that the $BW_{\rm s}$ should exceed 1.4 GHz and each stage should have a gain of approximately 5.25 dB. Therefore, considering the gain bandwidth and noise figure, the CGS which contains four the same gain stages is designed in the paper.

3.1 Active inductor

The element structure of the main amplifier is the fully differential cascaded stage. However, it is hard to achieve such a wide bandwidth based on CMSC 0.5 μm CMOS process. The active inductor technique is adopted to alleviate the bandwidth degradation, because the spiral inductor with a high inductance will occupy a lot of area and it is difficult to implement in CMOS process[12]. Fig. 4 shows the structure of the proposed CGS with an active inductor load.

The simplified small-signal analysis model of the active inductor load, which consists of a MOS transistor M_4 and a resistor $R_{\rm g}$, is shown in Fig. 5. Usually, there are $C_{\rm gs4}\geq C_{\rm gd4}$, $C_{\rm gs4}\geq C_{\rm ds4}$ and $g_{\rm m4}\geq g_{\rm ds4}$, so that the $C_{\rm gd4}$, $C_{\rm ds4}$, $g_{\rm ds4}$ can be neglected.

The equivalent impedance of the active inductor can be given as following[13]:

$$Z_{\rm in}=\frac{1+R_{\rm g}sC_{\rm gs4}}{g_{\rm m4}+sC_{\rm gs4}} \quad , \tag{5}$$

where $Z_{\rm in}$ is the output impedance. $C_{\rm gs4}$ is the gate-source capacitance of MOS transistor, and $g_{\rm m4}$ is the trans-conductance of MOS transistor. Therefore, the equivalent inductance L and resistance R can be calculated as following[14]:

$$L=\frac{\dfrac{R_{\rm g}}{\omega_{\rm T}}+\dfrac{1}{g_{\rm m4}\omega_{\rm T}}}{1+\left(\dfrac{\omega}{\omega_{\rm T}}\right)^2} \quad , \quad R=\frac{R_{\rm g}\left(\dfrac{\omega}{\omega_{\rm T}}\right)^2+\dfrac{1}{g_{\rm m4}}}{1+\left(\dfrac{\omega}{\omega_{\rm T}}\right)^2} \quad . \tag{6}$$

The $\omega_{\rm T}$ is the unity current gain angular frequency. In order to avoid undesirable peaking on the frequency response, the resistance $R_{\rm g}$ should be designed carefully according to the capacitive load of the following stage. The active inductors perform an impedance of $R_{\rm g}$ at low frequency. When the frequency is sufficiently high, the inductor L is formed by $R_{\rm g}$ and $C_{\rm gs4}$ so that the impedance of the gain stage is increased. The impedance change is similar to the inductor and the frequency within a certain range[15]. The gain of the common source amplifier that has a structure of the active inductor load can be expressed as following (7):

$$A_{\rm V}=\frac{g_{\rm m2}}{g_{\rm m4}}=\sqrt{\frac{W_2/L_2}{W_4/L_4}} \quad . \tag{7}$$

The formula reveals that the stage's gain only has received the influences on the dimension of the input and load transistors. Consequently, the circuit that uses the active inductor structure has stronger capacity against to the alteration of temperature and process. Besides, the formula can be obtained as (8):

$$\frac{V_{\rm out}}{V_{\rm in}}(s)=\frac{g_{\rm m2}(1+sR_{\rm g}C_{\rm gs4})}{g_{\rm m2}+sC_{\rm L}+s^2C_{\rm L}R_{\rm g}C_{\rm gs4}} \quad . \tag{8}$$

Through choosing the appropriate value of the L and R, the bandwidth can be extended largely while maintaining a suppressed gain peak over the frequency range. In summary, based on the above formula, the CGS that consists of four identical gain stages and active inductive load is the optimized choice for this design.

3.2 Inter-stage bandpass filter

During chip fabrication, many non-ideal elements such as the asymmetry layout design and slight deviations in MOS transistor will result in DC offset, especially for

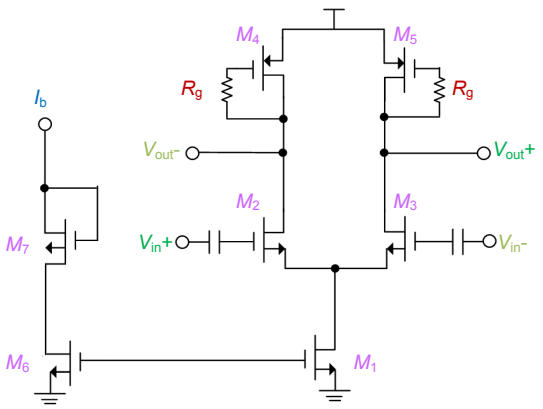

Fig. 4 The amplifier structure with active inductor technique

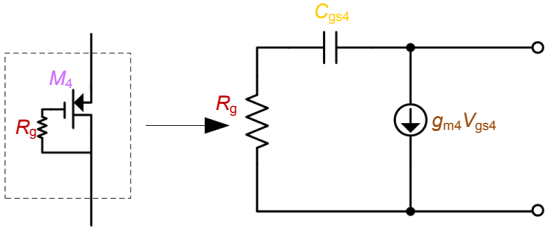

Fig. 5 Small-signal model of an active inductor

cascaded differential gain structure. Since the amplifier that uses the multi-stage cascade structure as a high gain, the DC offset voltage which generated by the preamplifier unit is amplified, resulting in a large shift of the operating point of the post amplifier[16]. Even if the input deviation is small, the amplification of the stages may cause the output buffer to reach the saturation.

In order to stabilize the operating point and DC gain, the structure of offset voltage compensation loop is required. This circuit employs capacitive coupling to eliminate DC offset. As shown in Fig. 6, C_1 and C_2 are DC blocking capacitors for eliminating DC offset. M_{a1}~M_{a8} (M_{b1}~M_{b8}) are NMOS transistors with the same substrate and source terminals to provide a self-bias voltage for the amplifier.

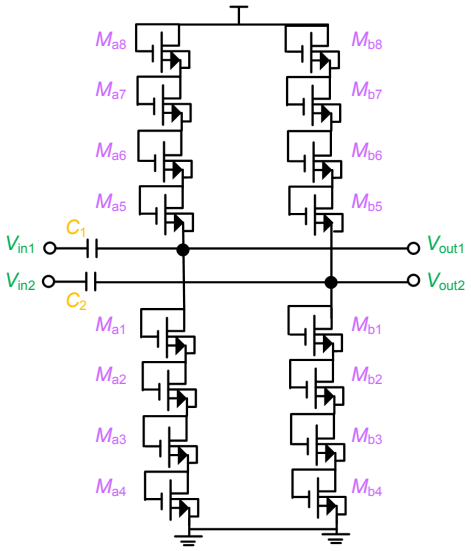

Fig. 6 The inter-stage bandpass filter of the schematic

Excessive bandwidth can cause additional noise to enter the receiver, which degrades the receiver's signal-to-noise ratio (SNR). Therefore, the bandwidth of the whole amplifier chains should be limited to a certain range. In order to meet the needs of the LADAR system, this work achieves an inter-stage bandpass filter by reusing the DC offset isolation circuit to mitigate the problem that the coupled capacitances occupy a lot of area in the CMOS process and lead to attenuate the signal. The simplified equivalent formula can be calculated as (9):

$$f_{\mathrm{L}}=\frac{1}{2\pi R_{\mathrm{g}}C_{\mathrm{s}}}\quad , \tag{9}$$

where f_{L} is the bandwidth of bandpass filter, R_{g} is the equivalent resistance of the NMOS transistors and C_{s} is C_1 and the parasitic capacitors of the NMOS transistors.

3.3 Output stage circuit

The output stage circuit is used to enhance the drive capability of the FDMA circuit, which includes two parts of modules. The large bandwidth amplifier (LBA) stage was employed before the output buffer (OB) to solve the problem that the parasitic capacitance causing by the large input transistors of OB results a reduction in bandwidth[17-18]. The architecture of the CGS circuit was adopted in the large bandwidth amplifier. It works as the former driver stage to eliminate the side effect of the output buffer. At last, the output buffer (OB) was designed to drive the PCB transmission lines and the load capacitance of the followed external circuit. As shown in Fig. 7, based on actual experience, the load resistors of the output buffer (OB) should be designed according to the actual situation and specific package.

4 Measure results

The proposed FDMA is fabricated in a CSMC 0.5 μm 2P3M Mixed CMOS technology. Fig. 8 shows the photograph of the fully differential main amplifier chip with an active area of 0.25 mm×0.25 mm, a core area of 0.16 mm×0.16 mm, and several extra pads were added for measurement. This chip consumes a power dissipation of 102.3 mW from 3.3 V voltage supply, in which the output buffer (OB) circuit consumes 73.2 mW. As shown in Fig. 9, the proposed chip was packaged in QFN40 and mounted on the test printed circuit board (PCB) and Fig. 10 displays the test apparatus and the environment.

The open loop gain and bandwidth of the proposed chip were measured by the Agilent vector network analyzer (E5071C)(Fig. 11).

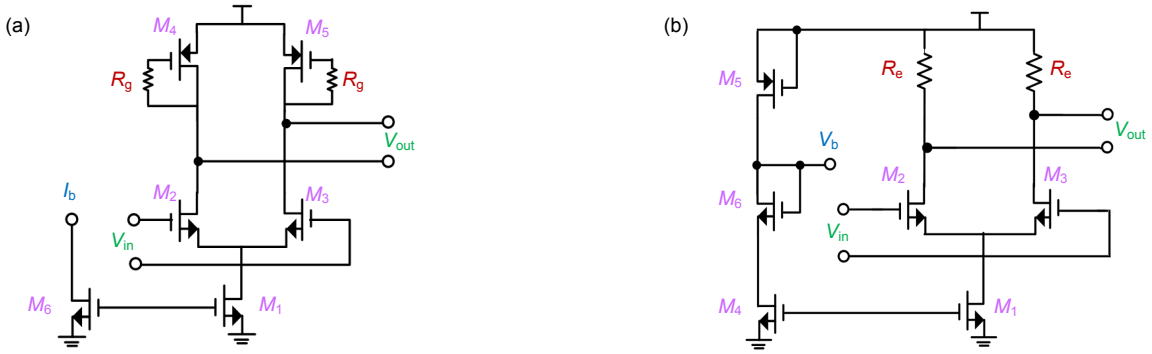

Fig. 7 The large bandwidth amplifier (a) and output buffer schematic (b)

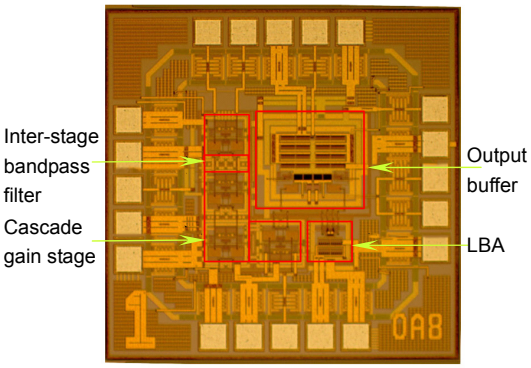

Fig. 8 Photograph of the fully differential main amplifier chip

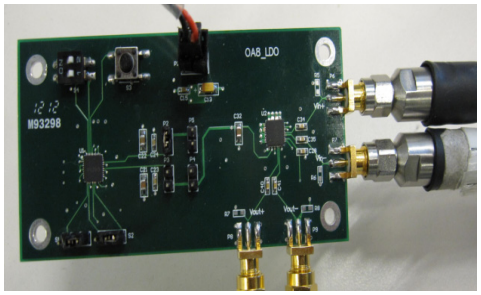

Fig. 9 PCB test board

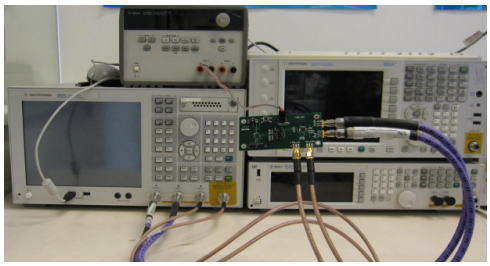

Fig. 10 Test apparatus and environment

From Fig. 11, it can be seen that the open loop gain of the chip is about 23.5 dB at 100 MHz, the -3 dB bandwidth is 730.6 MHz. The -3 dB bandwidth is limited to a certain range, in order to adapt the demand of the LADAR system.

Figure 12 shows the measured noise spectrum from the Agilent spectrum analyzer (N9020MAX). The input-referred noise voltage of the amplifier is 2.7 nV/sqrt(Hz) at 100 MHz with the 50 Ω input.

As shown in the Fig. 13, the measured response of the FDMA with the power 1 μW and 3 ns pulse width input in the system from the Tektronix Oscilloscope 5104B. The Fig. 14 illustrates the measured frequency response of the FDMA with the laser pulse frequency 10 kHz.

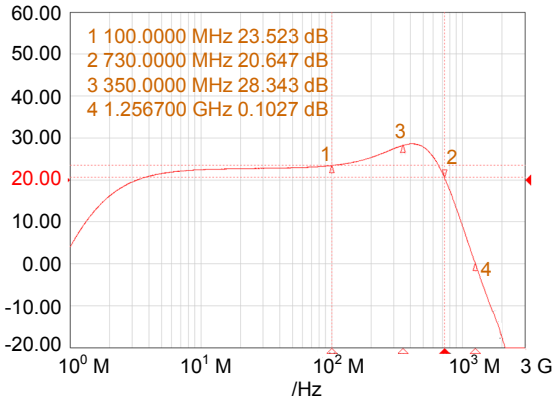

Fig. 11 Measured S parameters with the inter-stage bandpass filter

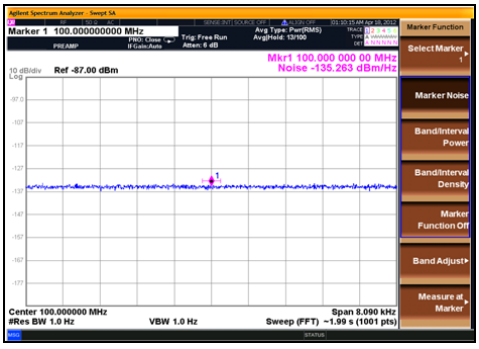

Fig. 12 Measured noise spectrum of the output

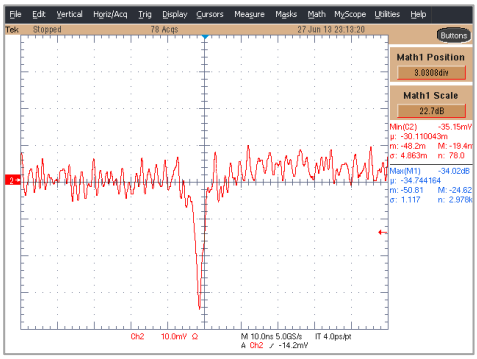

Fig. 13 Measured amplitude response of the FDMA

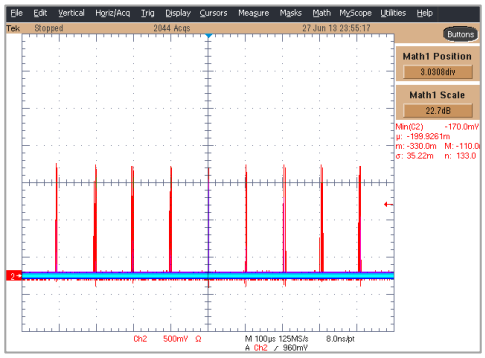

Fig. 14 Measured frequency response of the FDMA

5 Conclusion

An integrated a fully differential main amplifier for pulsed TOF imaging LADAR system with high bandwidth and low noise has been proposed and fabricated in CSMC 0.5 μm CMOS technology. The FDMA includes proposed cascaded gain stages, which enhance wide bandwidth performance, a large bandwidth amplifier (LBA) and an output buffer (OB) and the bandpass filter. The four levels cascaded architecture and active inductor technology are used to overcome the inadequate bandwidth problem and reduce the chip area under conventional process. By using the inter-stage bandpass filter, the -3 dB bandwidth is limited to improve the SNR, in order to meet the demand of the LADAR system. The measurement results have confirmed that the proposed FDMA chip achieves the -3 dB bandwidth of 730.6 MHz, and an open loop gain of 23.5 dB with the bandpass filter worked. The input-referred noise voltage is 2.7 nV/sqrt(Hz), which effectively reduces the system noise. This chip that occupies 0.25 mm×0.25 mm area consumes a power dissipation of 102.3 mW from the 3.3 V power supply. As a part of the integrated chip of the laser radar system, it can better meet the requirements of system.

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A high-performance CMOS FDMA for pulsed TOF imaging LADAR system

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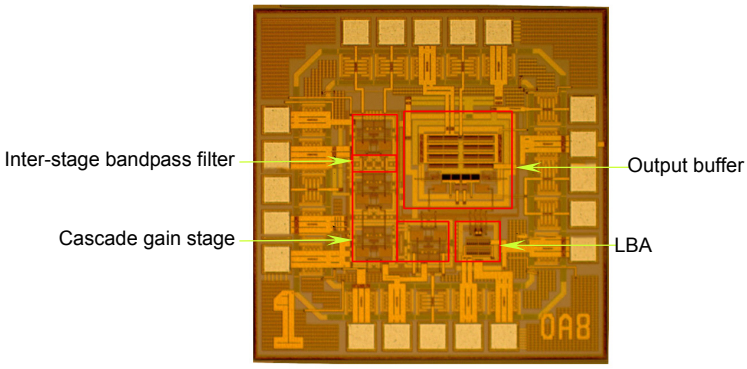

Photograph of the fully differential main amplifier chip

Overview: As an active optical remote imaging technology, the laser detection and ranging (LADAR) system shows an enormous potential in industrial and civil applications with the rapid development of unmanned aerial vehicle (UAV), and so on. Recently, LADAR are constantly developing towards integration, miniaturization and arraying in order to achieve higher detection and wider range of application. For the whole detection system, the performance height of the receiver circuit can directly determine the application height of the system. The amplifier receiver of the LADAR system which converts the small optical pulse signal into an electrical pulse mainly includes two parts: a photoelectric detector and the analog front-end circuits. Since the transmit power of the pulse laser are limited and considering the safety of human eyes, in active imaging systems the performance of the amplifier receiver becomes a critical issue. Therefore, a high-performance main amplifier is a key component to the LADAR system. This paper presents a high bandwidth and low noise fully differential main amplifier (FDMA) for the pulsed time-of-flight (TOF) imaging laser detection and ranging application, which is used to amplify the small pulse echo signal. To meet the entire system bandwidth requirements, the four levels cascaded architecture and active inductor technology are designed to enlarge the bandwidth of the circuit and reduce the chip area. The cascaded gain stages, which adopted DC offset isolation circuit, are more robust to the alteration of process and temperature compared to the traditional structure. A large bandwidth amplifier (LBA) and an output buffer (OB) structure has been designed to enhance the drive capabilities. Besides, in order to adapt the demand of the LADAR system, the amplifier receiver's bandwidth has been limited to improve the SNR by use of the inter-stage bandpass filter which reuses the DC offset isolation circuit. For the temperature variation of -40 ℃ to 85 ℃, the simulated results have confirmed the performances of the high bandwidth and low noise fully differential main amplifier. The proposed design was implemented and fabricated in CSMC CMOS technology. The measurement results show that the chip realizes the -3 dB bandwidth of 730.6 MHz, and an open loop gain of 23.5 dB with the bandpass filter worked. The input-referred noise voltage is 2.7 nV/sqrt(Hz), which effectively reduces the system noise. This chip that occupies 0.25 mm×0.25 mm in area consumes a power dissipation of 102.3 mW from the 3.3 V power supply. As a part of the integrated chip of the laser radar system, it can better meet the requirements of system and it shows good performance.

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